RESOLVING CAPACITOR DISCREPANCIES BETWEEN LARGE AND SMALL SIGNAL FET MODELS

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ABSTRACT

A novel solution is presented for the well known capacitor discrepancy problem between large and small signal FET models. The discrepancy arises due to the two-parameter bias voltage dependence of the intrinsic FET model capacitances. The resolution is enabled by the proper choice of partial-integration constants associated with the transformation of a charge source in the large signal model to a capacitor in the small signal model.

INTRODUCTION

Most large signal (i.e. nonlinear) models are generated from the use of small signal S-parameter data at various bias points in the I-V plane. From the S-parameter data, small signal linear models (Figure 1) at each bias point are commonly obtained using direct extraction procedures [1,2]. The variations of each element in the small signal model with respect to gate and drain bias voltage are then implemented in a large signal model. However, one of the major problems associated with this procedure is the discrepancy that occurs when attempting to regenerate the original small signal model at each bias from the large signal model.

This paper focuses on resolving the discrepancy caused by the two-parameter bias dependence of the capacitors in the model. Specifically, C_{gs}, C_{ds}, and C_{gd} of the small signal model are known to be functions of both gate and drain bias voltages [3]. That is, each of the three capacitors in the model depends on the voltage across its own terminals and the voltage across a remote set of terminals.

THEORY

The generalization of a capacitor in a small signal model is a charge source in a large signal model [4]. To determine the charge source that will model the effects of each capacitor, recall that the definition of capacitance is given by

$$Capacitance \equiv \frac{dQ}{dV} \qquad (1)$$

where Q is the charge on the capacitor terminals and V is the voltage difference between the two terminals. Since capacitors in the FET model are functions of two voltages, the above equation can be written as

$$C(V_L, V_R) \equiv \frac{\partial Q(V_L, V_R)}{\partial V_L} \qquad (2)$$

where V_L and V_R are defined as the voltage across the capacitor's terminals (local voltage) and the voltage across a remote set of terminals (remote voltage), respectively.

By integrating equation (2), it can be seen how each bias dependent capacitor $C(V_L,V_R)$ in the small signal model (Figure 2a) is used to generate a corresponding charge source $Q(V_L,V_R)$ for the large signal model (Figure 2b). The result is

$$Q(V_L, V_R) = \int_0^{V_L} C(\xi, V_R)\, d\xi + Q_o(V_R) \qquad (3)$$

Note that the process of partial integration has introduced a new function Q_o that is only dependent on the remote voltage. Theoretically, Q_o equals the charge on the capacitor when the local voltage is zero. As will be shown later, Q_o is the key to resolving the discrepancy that occurs when attempting to regenerate the original small signal models (at each bias) from the large signal model.

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Note that the current flowing through the small signal capacitor (Figure 2a) is given by the familiar form

$$i_C = C(V_L, V_R)\frac{dV_L}{dt} = \frac{\partial Q(V_L, V_R)}{\partial V_L}\frac{dV_L}{dt} \quad (4)$$

However, regardless of the amplitude of the incoming signal, the current flowing through the charge source (Figure 2b) in the large signal model is given by

$$i_Q = \frac{dQ(V_L, V_R)}{dt} = \frac{\partial Q(V_L, V_R)}{\partial V_L}\frac{dV_L}{dt} + \frac{\partial Q(V_L, V_R)}{\partial V_R}\frac{dV_R}{dt} \quad (5)$$

This results in the small signal model shown in Figure 2c where a new element called a "transcapacitor" is unavoidably introduced [4,5]. The transcapacitance (C_T) is described by

$$C_T(V_L, V_R) \equiv \frac{\partial Q(V_L, V_R)}{\partial V_R} \quad (6)$$

Note that the transcapacitance causes the discrepancy between the capacitor in Figure 2a of the original small signal model and the linearization of the corresponding charge source displayed in the network in Figure 2c. To eliminate this discrepancy, it is desired that

$$i_C = i_Q \quad (7)$$

From equations (4) and (5), the above condition can be satisfied by setting the transcapacitance equal to zero. That is

$$C_T \equiv \frac{\partial Q(V_L, V_R)}{\partial V_R} = 0 \quad (8)$$

Substituting from equation (3) yields

$$\frac{\partial}{\partial V_R}\left[\int_0^{V_L} C(\xi, V_R)\, d\xi\right] + \frac{\partial Q_o(V_R)}{\partial V_R} = 0 \quad (9)$$

For a preselected value of $V_L=V_{LO}$, the above equation can be satisfied identically (as a function of V_R) by the choice

$$Q_o(V_R) = -\int_0^{V_{LO}} C(\xi, V_R)\, d\xi \quad (10)$$

With this choice of Q_o, the effects of the transcapacitance are removed from the charge source for, and presumably near, the local voltage value $V_L=V_{LO}$. As a result, the discrepancy that occurs when attempting to regenerate the original bias dependent small signal models from the nonlinear model has effectively been finessed.

THEORY VERIFICATIONS

To verify the above solution of the capacitor discrepancy problem, a comparison was made between S-parameters generated from small and large signal models for an example 0.5µm x 300µm MESFET device. Based on element values extracted from measured S-parameters, functions were generated describing the bias dependent capacitors C_{gs}, C_{gd}, and C_{ds} of the simplified small signal model of Figure 3 [3]. An expression was also generated from pulsed I-V data to describe the current source I_{DS} [6], the derivatives of which are used to determine the transconductance g_m and output conductance g_{ds} (see Figure 3). The large signal model of Figure 4 was constructed by using the aforementioned I_{DS} expression, and integrating the capacitor functions using equation (3) to obtain the charge sources Q_{gs}, Q_{gd}, and Q_{ds}. In doing this last step, two approaches were used. The first approach incorporates the new capacitor resolution described by equation (10) to assign Q_o, and the second approach ignores Q_o ($Q_o=0$). The models were implemented in HP-EESOF's Libra™ CAD software, and the following three cases were compared:

Case I (denoted by SSM) corresponds to the small signal model evaluated at $V_{gs}=-0.5V$, $V_{gd}=-5.5V$, and $V_{ds}=5.0V$ (see Figure 3).

Case II (denoted by LSM1T0) corresponds to the large signal model shown in Figure 4 with the transcapacitance set equal to zero by selecting Q_o according to Equation (10) where V_{LO} is -0.5, -5.5, and 5.0 for Q_{gs}, Q_{gd}, and Q_{ds}, respectively.

Case III (denoted by LSM1T) corresponds to the large signal

model shown in Figure 4 with Q_o arbitrarily set equal to zero (which corresponds to a non-zero transcapacitance).

For Case I, S-parameters were generated using linear nodal analysis. For cases II, and III, S-parameters were generated by low power (-60dBm) Harmonic Balance simulations of the large signal models.

Figures 5 through 8 compare the simulations of the small and large signal models. The results show that the large signal model that uses equation (10) for Q_o regenerates all four S-parameters of the small signal model perfectly. On the other hand, the large signal model that ignores Q_o fails to regenerate accurately the S-parameters of the small signal model.

Further testing suggests that the proper choice of Q_o improves the convergence of Harmonic Balance simulations of large signal models. For the example device, when the input signal went above 14 dBm, the Harmonic Balance analysis failed to converge for the model with Q_o equal to zero (LSM1T). In contrast, harmonic balance analysis of the model that uses equation (10) for Q_o (LSM1T0) converged to a solution through 26 dBm of input power.

CONCLUSION

To summarize, a precise method of dealing with two-parameter bias dependent capacitors has been formulated such that the large signal model accurately tracks small signal model performance. Furthermore, the method appears to improve the convergence of Harmonic Balance simulations of large signal FET models.

REFERENCES

[1] M. Berroth and R. Bosch, "Broad-Band Determination of the FET Small-Signal Equivalent Circuit," IEEE Trans. Microwave Theory and Tech., vol. MTT-38, pp. 891-895, July 1990.

[2] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A New Method for Determining the FET Small-Signal Equivalent Circuit," MTT-36, pp. 1151-1159, July 1988.

[3] M. Calvo, Ph.D. Dissertation, University of South Florida, In preparation.

[4] D. Root and B. Hughes, "Principles of Nonlinear Active Device Modeling for Circuit Simulation," 32nd ARFTG Conference, December 1988.

[5] A.D. Snider, "Charge Conservation and the Transcapacitance Element: An Exposition," IEEE Transaction on Education, Accepted for publication.

[6] M. Calvo, P. Winson, A. Snider, and L. Dunleavy, "A More Robust I_{DS} Equation for FET Modeling," In preparation.

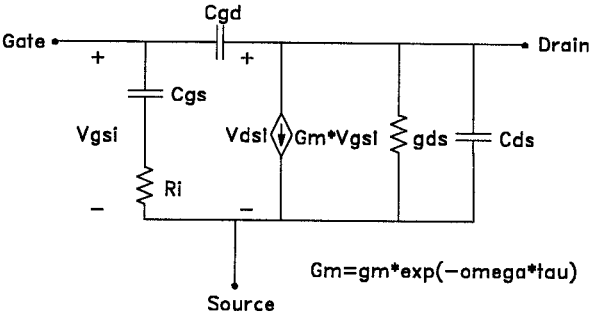
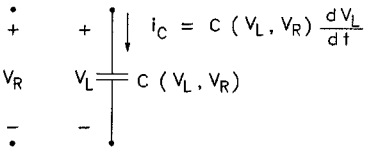
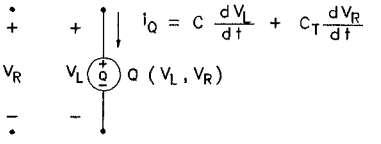


Figure 1: "Industry-standard" small signal intrinsic model for the MESFET.

2a) Small signal model capacitor at each bias.



2b) Large signal model charge source.



2c) Linearization of a charge source.

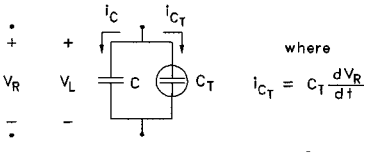


Figure 2: Discrepancy caused by the linearization of the charge source.

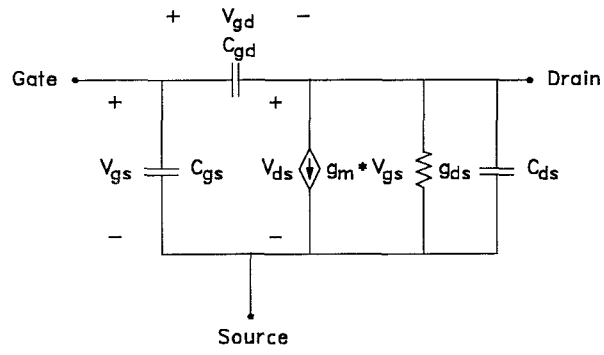


Figure 3: Simplified small signal intrinsic model for the MESFET.

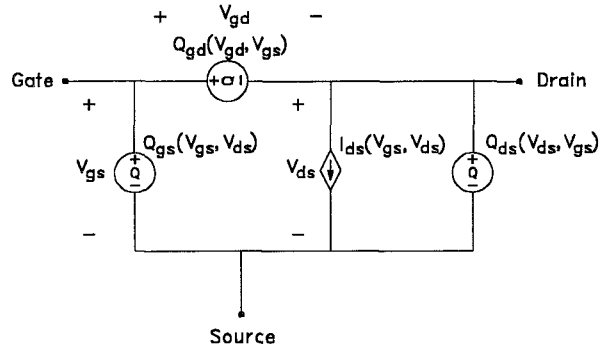


Figure 4: Simplified large signal intrinsic model for the MESFET.

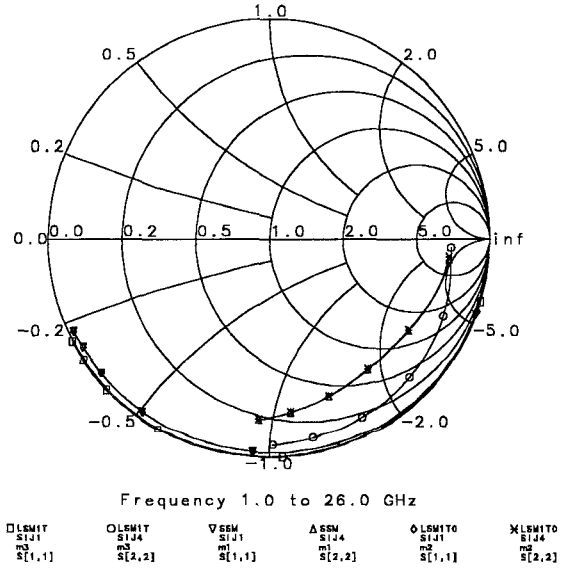


Figure 5: S11 and S22 for the small signal model (SSM), the large signal model with proposed Q_o (LSM1T0), and the large signal model with Q_o=0 (LSM1T).

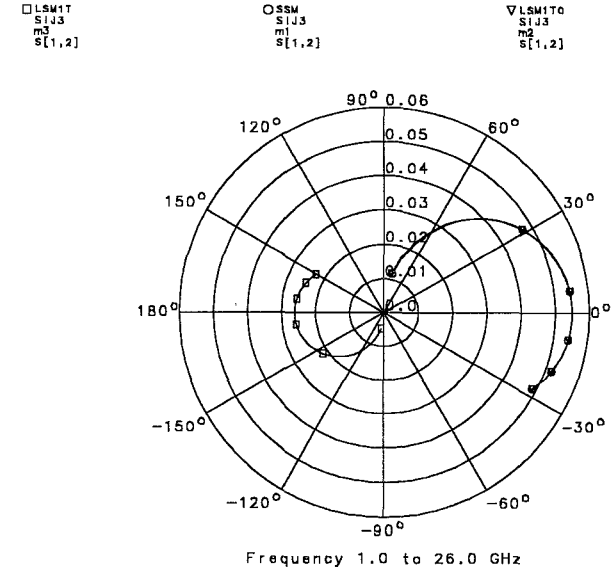


Figure 6: S12 for the small signal model (SSM), the large signal model with proposed Q_o (LSM1T0), and the large signal model with Q_o=0 (LSM1T).

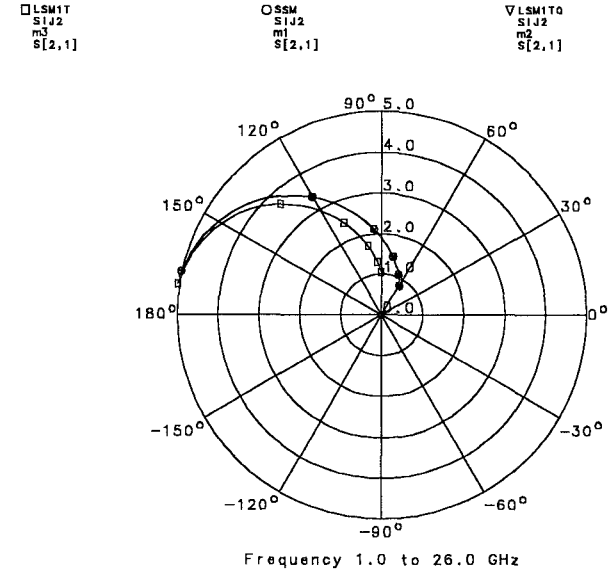


Figure 7: S21 for the small signal model (SSM), the large signal model with proposed Q_o (LSM1T0), and the large signal model with Q_o=0 (LSM1T).